**Lab report no 1**



**Fall 2022**

**CSE-308L Digital Systems Design Lab**

**Submitted By**

**Names Registration No**

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Section: **A**

**Date**:4,2,22

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**Lab tasks:**

**1- Implement a buffer at the gate level.**

**2- Implement an inverter at the gate level.**

**Code for both buffer and inverter: -**

module circuit(A,nb,nt);

input A;

output nb,nt;

buf b1(nb,A);

not n1(nt,A);

endmodule

module lab1task1();

reg A;

wire nb,nt;

circuit cr(A,nb,nt);

initial

begin

$display ("A nb nt");

A=0;

#10 $display("%b %b %b",A,nb,nt);

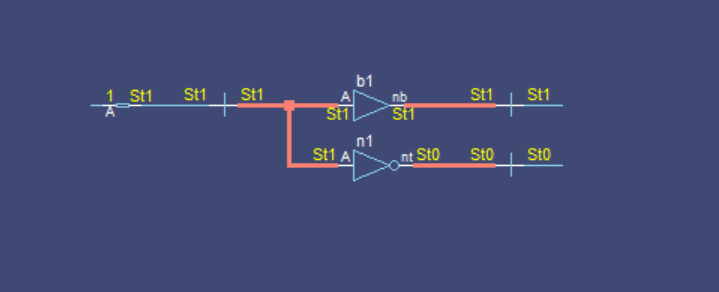
A=1;

#10 $display("%b %b %b",A,nb,nt);

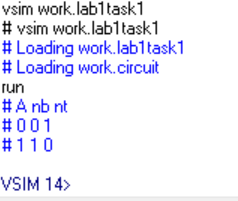
end

endmodule

**Design Hardware: -**

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**Run Project: -**

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**3- Implement an OR gate using a NAND gates.**

module circuit(z,x1,x2);

input x1,x2;

output z;

wire y1,y2;

nand a1(y1,x1);

nand a2(y2,x2);

nand a3(z,y1,y2);

endmodule

module stimlab1orfromnand();

reg x1,x2;

wire z;

circuit cr(z,x1,x2);

initial

begin

$display ("x1 x2 z");

x1=0; x2=0;

#10 $display("%b %b %b",x1,x2,z);

x1=0; x2=1;

#10 $display("%b %b %b",x1,x2,z);

x1=1; x2=0;

#10 $display("%b %b %b",x1,x2,z);

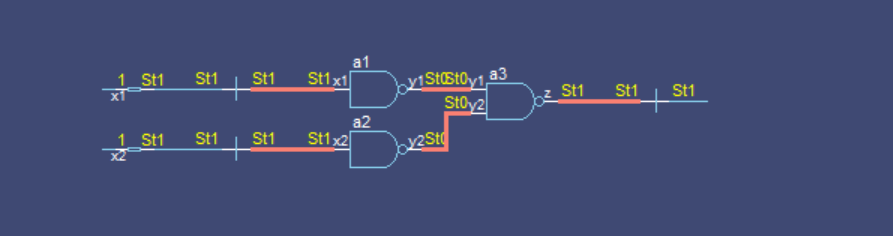
x1=1; x2=1;

#10 $display("%b %b %b",x1,x2,z);

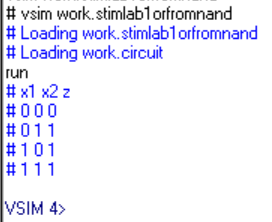
end

endmodule

**Design Hardware: -**

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**Run Project: -**

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**4- Implement the following equation where z is output and x1, x2, x3, x4, and**

**x5 are inputs of the circuit.**

**z = ( y1 + y2 )’**

**y1 = x1.x2**

**y2 = (x3.x4.x5)**

**code:**

module circuit(z,x1,x2,x3,x4,x5);

input x1,x2,x3,x4,x5;

output z;

wire y1,y2;

and a1(y1,x1,x2); //y1=x1 + x2

and a2(y2,x3,x4,x5); //y1=x3 + x4 + x5

not n1(ny2,y2);

or o1(y,y1,ny2);

not n2(z,y); //z=(y1 + y2)'

endmodule

module stimlab1task4();

reg x1,x2,x3,x4,x5;

wire z;

circuit cr(z,x1,x2,x3,x4,x5);

initial

begin

$display ("x1 x2 x3 x4 x5 z");

x1=0; x2=0; x3=0; x4=0; x5=0;

#10 $display("%b %b %b %b %b %b",x1,x2,x3,x4,x5,z);

x1=0; x2=0; x3=0; x4=0; x5=1;

#10 $display("%b %b %b %b %b %b",x1,x2,x3,x4,x5,z);

x1=0; x2=0; x3=0; x4=1; x5=0;

#10 $display("%b %b %b %b %b %b",x1,x2,x3,x4,x5,z);

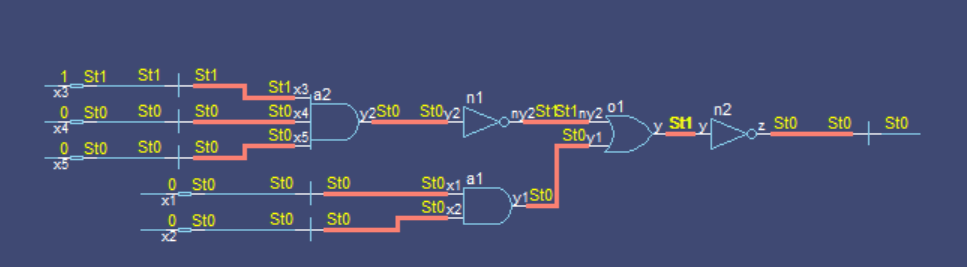
x1=0; x2=0; x3=1; x4=0; x5=0;

#10 $display("%b %b %b %b %b %b",x1,x2,x3,x4,x5,z);

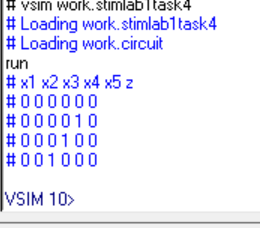
end

endmodule

**Design Hardware: -**

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**Run Project: -**

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